SMALL FORM FACTOR COGNITIVE RADIO, IMPLEMENTED VIA FPGA PARTIAL RECONFIGURATION, REPLACING A WIRED VIDEO TRANSMISSION SYSTEM

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INTRODUCTION

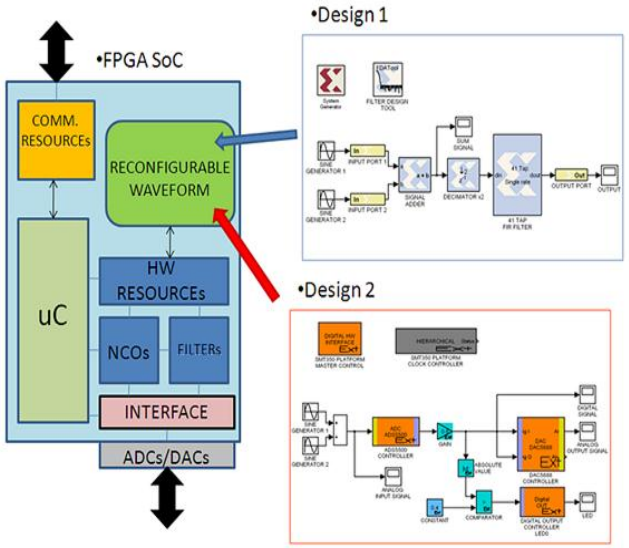
- Motivation
  - Trend towards reduction/no inclusion of new wires
  - Specially appreciated in industrial environments (also in airplanes, trains, vertical transport)
  - Harsh environments

Suitable characteristics for
Software Defined Radios / Cognitive Radios

- Selected application
  - Video transmission (e.g. CCTV)
    - Data transmission + reliability

INTRODUCTION

Design framework:



Rapid prototyping tools

- · Graphical programming, no code writing.
- · Early functional simulations
- ·Easy debugging

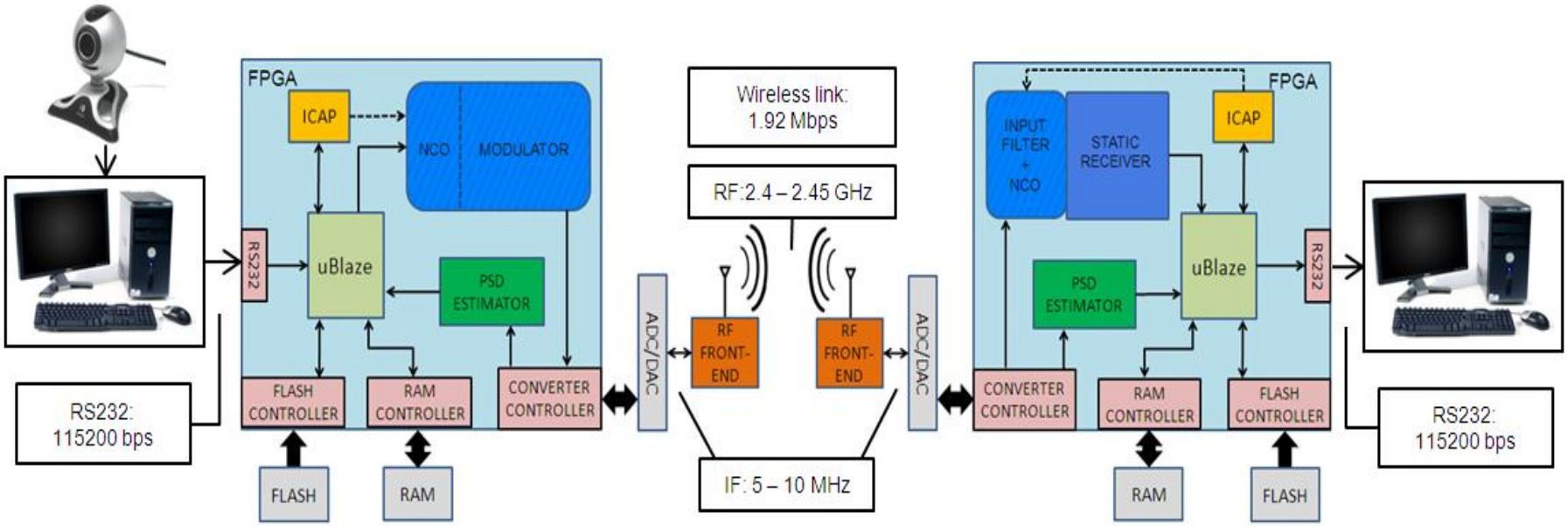
- Communication system where a single piece of hardware has different functionalities in different times

Fit perfectly

FPGA partial reconfiguration (PR)

- · Design flexibility
- · Hardware reuse.
- · Power save

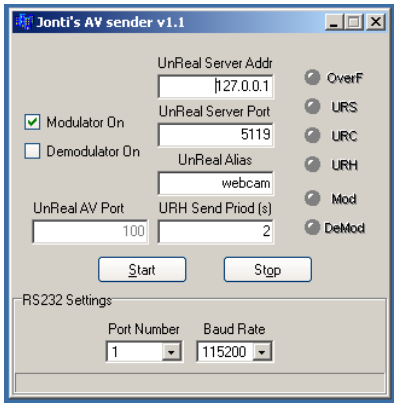
OVERALL VIEW



- Webcam + PCs + RS232 link
- Replacement by a FPGA based, custom, cognitive, wireless link

OVERALL VIEW

- Software for video streaming
  - AV RS232 Sender by Olds [1]
  - Raw capture: 208x170 pixels (828 kbps)
  - VC1(WMV9) compression (90kbps)



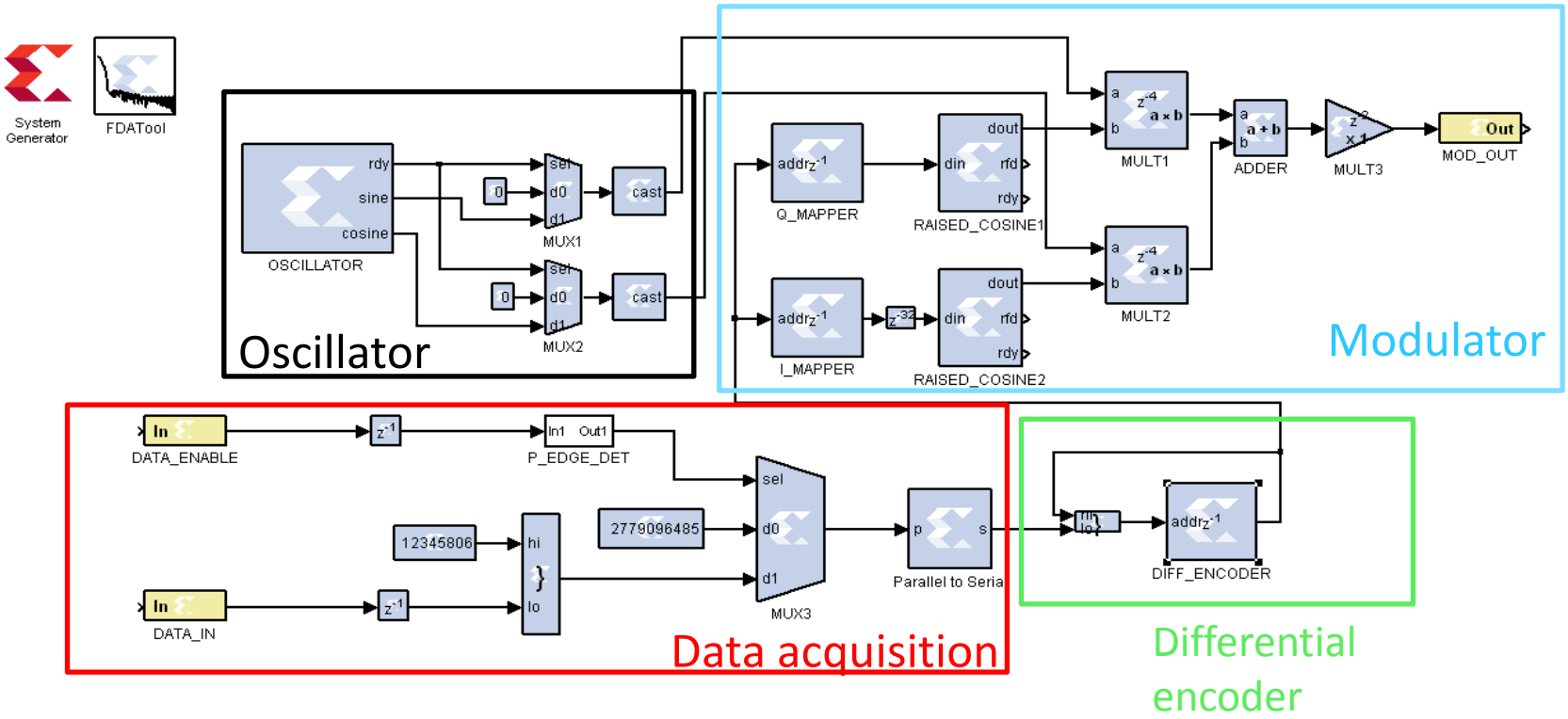
- Hardware platform
  - Two SMT8096 boards from Sundance
  - Virtex 4-SX (XCV4SX35) FPGA
  - ADC: 14 bit @ 125 MHz (set to 61.44 MHz)
  - DAC: 16 bit @ 500 MHz (set to 61.44 MHz)

[1] http://homepages.paradise.net.nz/peterfr2/avrs232sender.htm

OVERALL VIEW

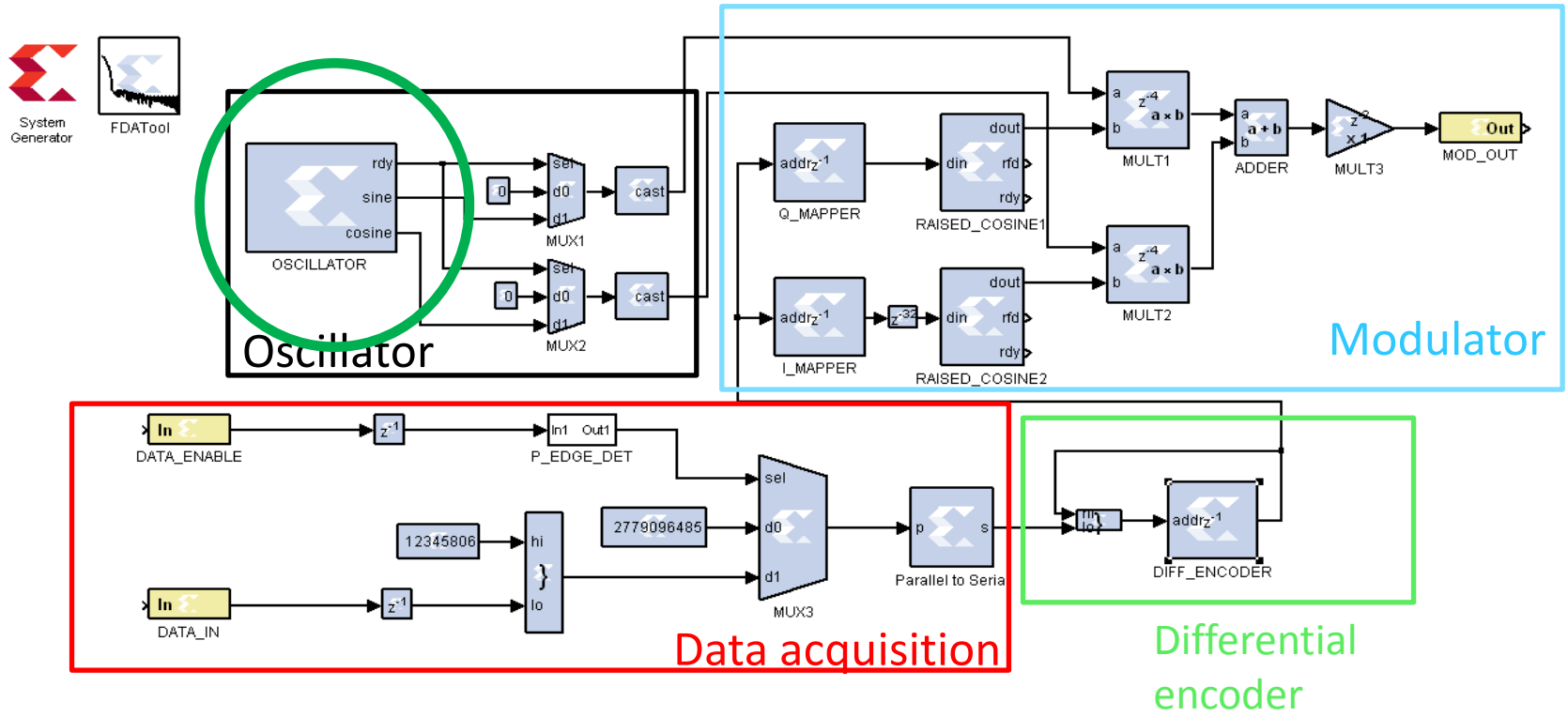
- RF Front end
  - Custom made front-ends
  - IF: 5 – 10 MHz
  - RF: 2.4 – 2.45 GHz
  - No reconfiguration
- Rapid prototyping tool
  - Xilinx's System Generator

TRANSMITTER



- Basic characteristics:
  - OQPSK modulation
  - 1.92 Mbps
  - FI: 5-10 MHz (PR implemented)
  - Output filter: 64 tap, 0.25 roll-off
  - 2 PR granularities (oscillator and complete)

TRANSMITTER



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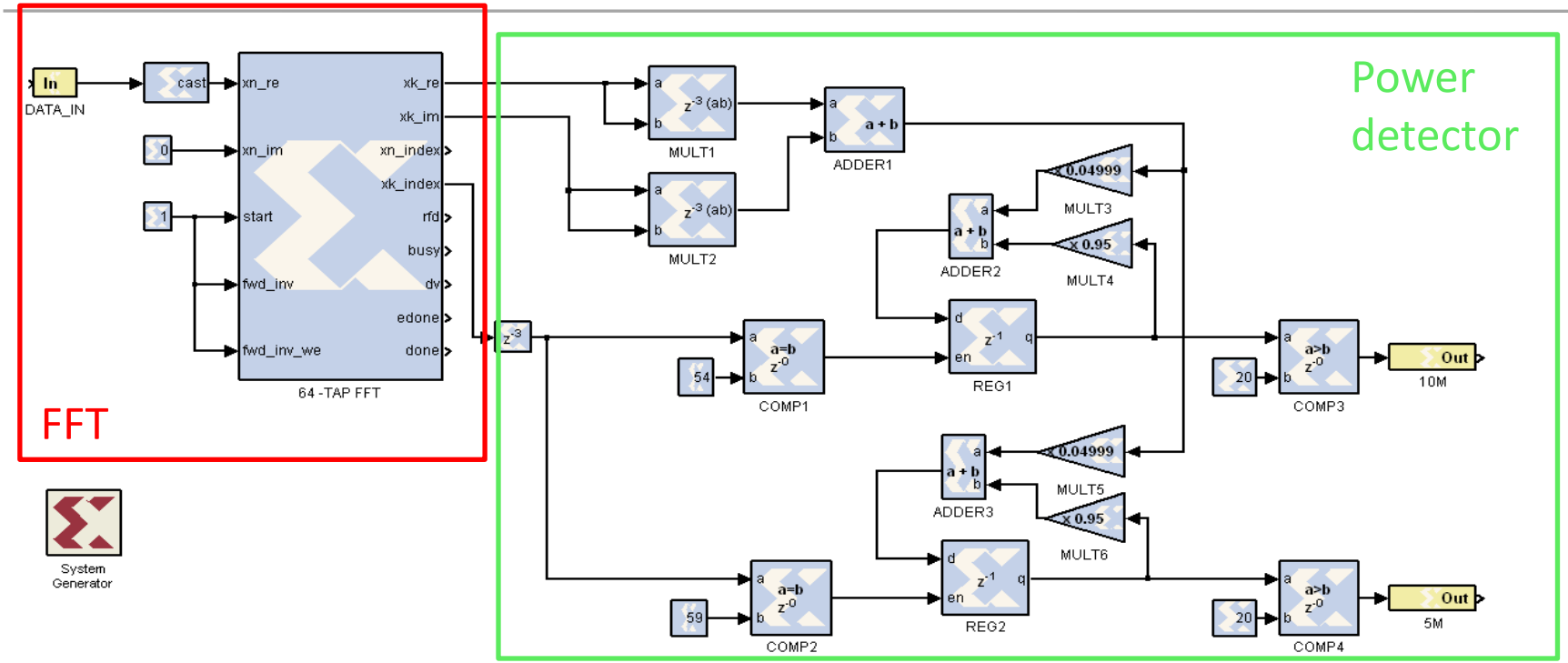
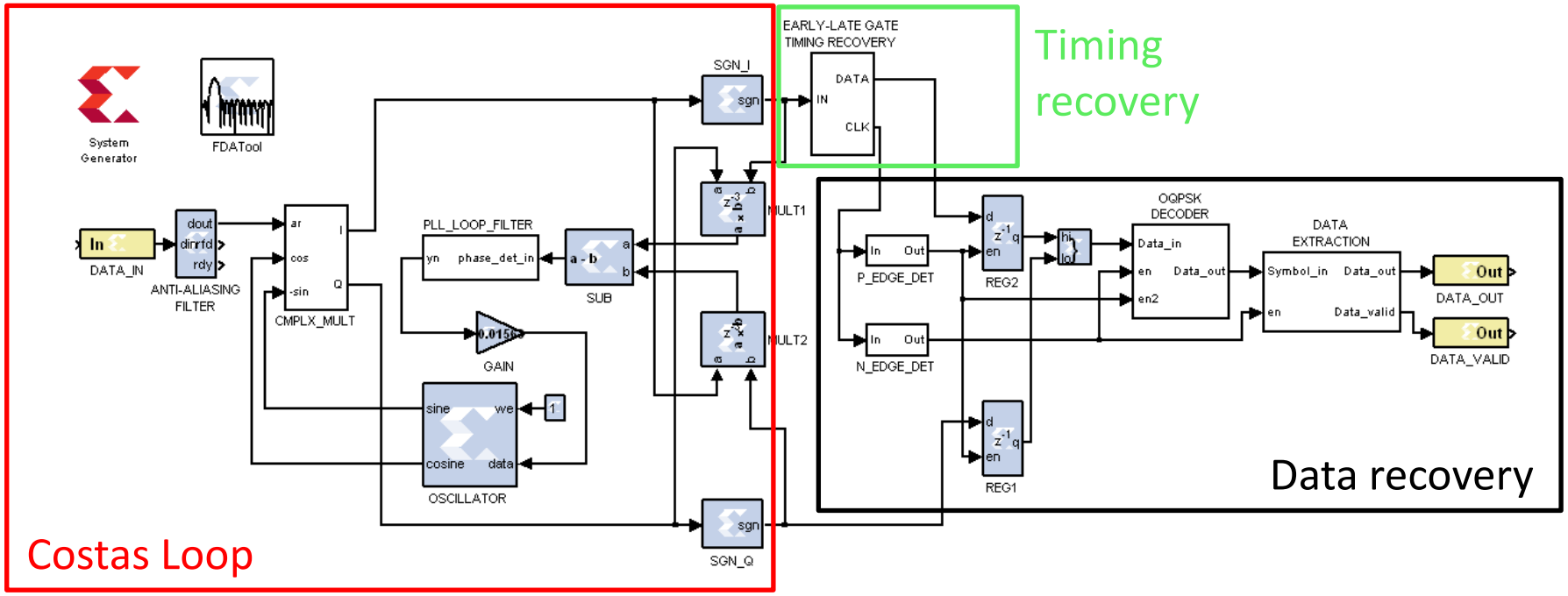
PSD ESTIMATOR



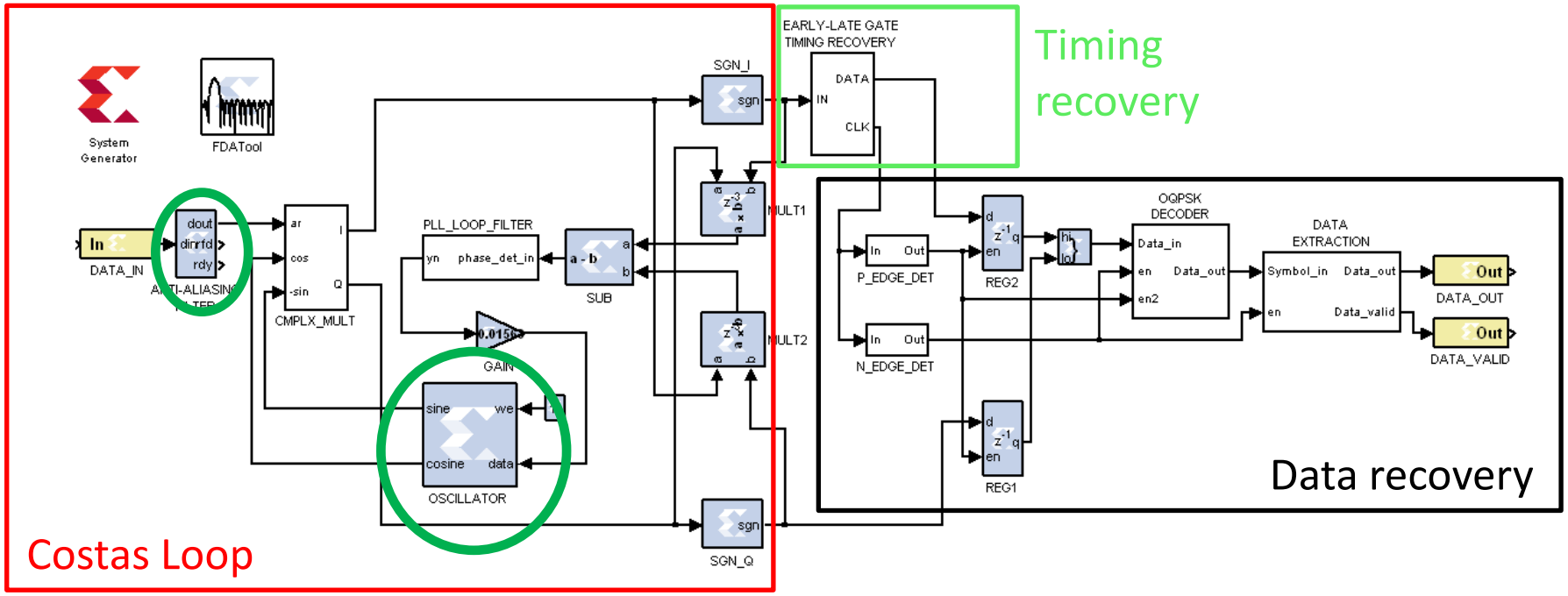
- Basic characteristics:
  - FFT: 64 tap
  - Fs: 61.44 MHz
  - Resolution: 1 MHz

RECEIVER



- Basic characteristics:
  - Carrier frequency and phase recovery via Costas loop algorithm
  - Timing recovery via early-late gate algorithm
  - Anti-aliasing filter and oscillator reconfiguration

RECEIVER



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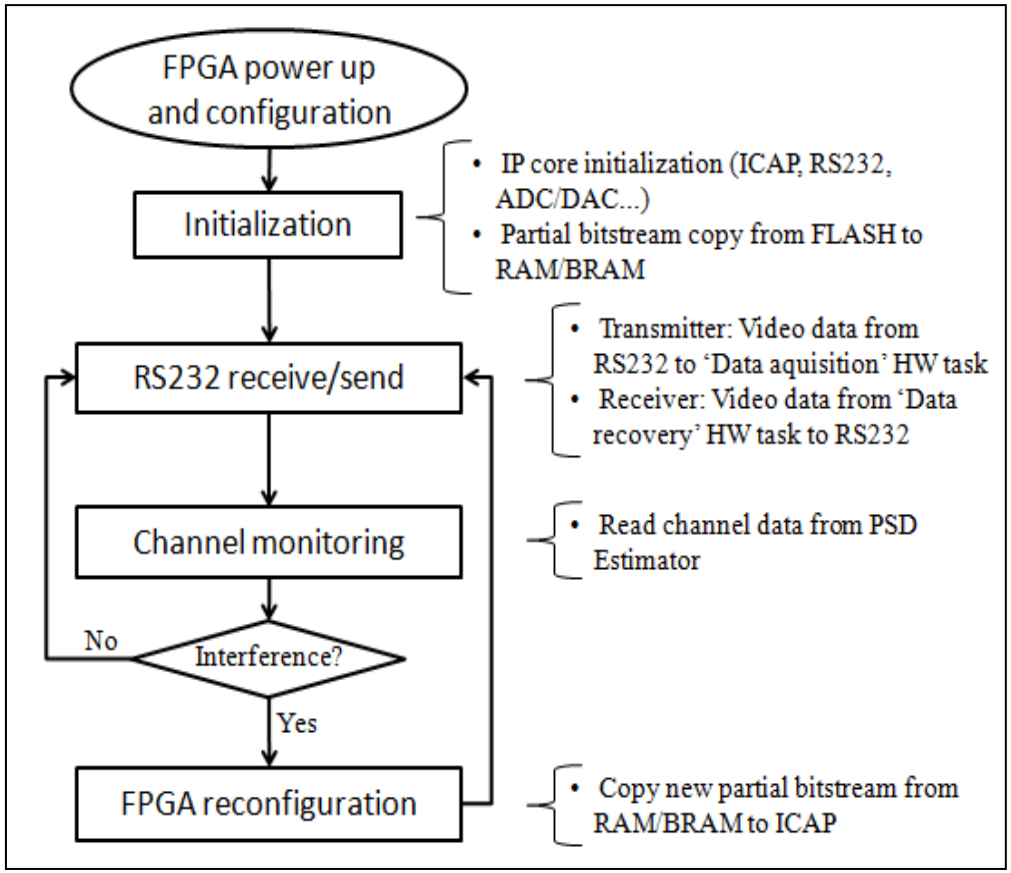
ARCHITECTURE FOR PARTIAL RECONFIGURATION

- Dynamic partial reconfiguration
  - Change part of the FPGA while the rest remains unaltered
    - FPGA resource saving
    - Power saving
- Architecture
  - Internal Configuration Access Port (ICAP)
  - MicroBlaze processor
    - ICAP controller
    - Frequency change control (PSD estimation)
    - RS232 communication
    - Initialization procedures

ARCHITECTURE FOR PARTIAL RECONFIGURATION

Software algorithm



MEASUREMENTS

FPGA resources

Transmitter FPGA resource utilization					
	SLICE	Flip-Flop	LUT	BRAM	DSP48
OQPSK Modulator	548 (4%)	644 (2%)	813 (3%)	3 (2%)	70 (36%)
Oscillator	51 (<1%)	61 (<1%)	79 (<1%)	1 (<1%)	0 (0%)
PSD estimator	1547 (10%)	1955 (6%)	2089 (7%)	3 (2%)	32 (17%)
uBlaze system	3074 (20%)	3004 (10%)	3943 (13%)	33 (17%)	3 (2%)
Full design	5432 (35%)	5679 (18%)	6881 (22%)	40 (21%)	105 (55%)
NR design	5531 (36%)	5772 (19%)	6988 (23%)	41 (21%)	105 (55%)

Receiver FPGA resource utilization					
	SLICE	Flip-Flop	LUT	BRAM	DSP48
Filter + oscillator	2183 (14%)	3158 (10%)	1928 (6%)	1 (<1%)	41 (21%)
Static receiver	1037 (7%)	1201 (4%)	982 (3%)	1 (<1%)	3 (2%)
PSD estimator	1547 (10%)	1955 (6%)	2089 (7%)	3 (2%)	32 (17%)
uBlaze system	3074 (20%)	3004 (10%)	3943 (13%)	33 (17%)	3 (2%)
Full design	8091 (53%)	9544 (31%)	9390 (31%)	38 (20%)	79 (41%)
NR design	10324 (67%)	13224 (43%)	11365 (37%)	39 (20%)	120 (63%)

- Small form factor: 35% and 53% of a “small” FPGA
- MicroBlaze is the biggest part (20%)
- Benefits of the partial reconfiguration

MEASUREMENTS

Reconfiguration time

Reconfiguration time			
	Partial bitstream size	Bitstream storage	
Design	-	RAM	BRAM
Transmitter (oscillator)	24 KBytes	4,5 ms	3 ms
Transmitter (whole)	267 KBytes	60 ms	-
Receiver (Filter and osc.)	763 Kbytes	171,5 ms	-

- Main partial reconfiguration disadvantage
- Two possibilities of bitstream storage
- ICAP theoretical speed: 400 MBps
- ICAP measured speed: 4.5 – 8 MBps
- Enhanced implementation: reconfiguration below the millisecond

CONCLUSIONS AND FUTURE WORK

- Conclusions
  - Simple application but valid as proof-of-concept
  - Partial reconfiguration enables area and power reduction at the expense of reconfiguration time.
  - Inefficient ICAP controller implementation.

- Future work
  - Improve the ICAP controller implementation
  - Apply this design framework to a communication with hard timing requirements (e.g. Ethernet)
  - Develop a complete reconfigurable chain (FPGA + front-end + antennas)

QUESTIONS